15th EUROMICRO Conference on Digital System Design

September 5-7, 2012
Çeşme, İzmir, Turkey
PROGRAM


Wednesday
05-sept-12
Thursday
06-sept-12
Friday
07-sept-12
Registration
Opening
Keynote 1: SEAA 1
Coffe Break
FTDSD_1
MORPS-1
SHES_1
Lunch Break
Keynote 2: DSD 1 F.Kurdahi, UC Irvine, CESC
FTDSD_2
ET_1
EPDSD-1
Coffe Break/ Poster Session P-1
MORPS_2
AHSA_1
EPDSD_2
Welcome
Registration
Keynote 3: DSD-2 R.Leupers
Coffe Break
FTDSD_3
SOC&NOC_1
EPDSD-3
Lunch Break
Keynote 4: : DSD-3 Rich Goldman, Synopsys
DTDS_1
ET_2
SHES_2
Coffe Break/ Poster Session P-2
FDR
DHCPS
EPDSD-4
Social Event
Registration
Keynote 5 : SEAA-2
Coffe Break/Poster Session P-3
AHSA_2
Appli_1
SoC&NoC_2
Lunch Break
AHSA_3
SLEO_WN_1
SMVT
Coffe Break/Poster Sesion P-4
SHES_3
SLEO_WN_2
DTDS_2
MSDA
Appli_2
WiP
Closing Session

AHSA	Architectures and Hardware for Security Applications
APP	Applications of (embedded) digital systems
DHCPS	Design of Heterogeneous Cyber-Physical Systems
DTDS	Dependability and Testing of Digital Systems
ET	Important issues introduced by Emerging technologies
EPDSD	European Projects in DSD
FDR	Flexible Digital Radio
FTDSD	Fault Tolerance in Digital System Design
MORPS	Monitoring and Reconfiguration of Parallel Systems
MSDA	Multicore Systems: Design and Applications
P	Poster Session
SHES	System, hardware and embedded software design and automatic synthesis.
SLEO_WSN	System Level Energy Optimization and Wireless Sensor Networks
SMVT	System, hardware and embedded-software specification, modeling, verification and test
SoC&NoC	Systems and Networks on Chip
WiP:	Work in Progress
LP*	Long Presentation (30 min)

* By default the presentation duration is 15 minutes.

Wednesday, 5 September 2012

8:30 – 9:30 Registration

9:30 – 10:00 Opening

Location: Ballroom

10:00 – 11:00 Keynote Speech – 1 (SEAA - 1)

Location: Ballroom

- Model-Driven Engineering and the Impact of a Change
  Alexander Egyed

11:00 – 11:30 Coffee Break

Location: Foyer

11:30 – 13:00 Sessions

FTDSD– 1: Fault Tolerance in Digital System Design

Location: Ballroom

Chair: Z. Kotasek

Impact of duty factor, stress stimuli, and gate drive strength on gate delay degradation with an atomistic trap-based BTI model, *[Best Paper Candidate],*
Halil Kukner, Pieter Weckx, Praveen Raghavan, Ben Kaczer, Francky Catthoor, Liesbet Van der Perre, Rudy Lauwereins and Guido Groeseneken

Architecture and Design Analysis of a Digital Single-Event Transient/Upset Measurement Chip [Best Paper Candidate],
Varadan Savulimedu Veeravalli, Ulrich Schmid, Andreas Steininger and Thomas Polzer

- Accurate Estimation of Leakage Power Variability in Sub-Micrometer CMOS Circuits *[Best Paper Candidate].*
  Omid Assare, Mahmoud Momtazpour and Maziar Goudarzi

MORPS– 1: Monitoring and Reconfiguration of Parallel Systems

Location: Gerence 2

Chair: P. Liljeberg

- ReMORPH -- A Runtime Reconfigurable Architecture
  Kolin Paul, Chinmaya Dash and Mansureh Moghaddam
- Designing a High Performance and Reliable Networks-on-Chip using Network Interface Assisted Routing Strategy
  Khalid Latif, Amir-Mohammad Rahmani, Tiberiu Seceleanu and Hannu Tenhunen

- A Scalable Monitoring Infrastructure for Self-Organizing Many-Core Architectures
  David Kramer and Wolfgang Karl

SHES– 1: System, Hardware and Embedded Software Design and Automatic Synthesis

Location: Gerence 3

Chair: A.Yurdukal

- On the design of configurable modulo 2^n±1 residue generators
  Constantinos Efstathiou, Nikos Moschopoulos, Kostas Tsoumanis and Kiamal Pekmestzi
- Projected Don't Cares
  Anna Bernasconi, Valentina Ciriani, Gabriella Trucco and Tiziano Villa
- SUT-RNS Residue-to-Binary Converters Design
  Evangelos Vassalos, Dimitris Bakalis and Haridimos Vergos

13:00 – 14:00 Lunch Break

14:00 – 15:00 Keynote Speech – 2 (DSD - 1)

Location: Ballroom

- Exploiting Error-Awareness in System Design
  Fadi J Kurdahi

15:00 – 16:00 Sessions

FTDSD – 2: Fault Tolerance in Digital System Design

Location: Ballroom

Chair: H. Kubatova

- Automated Generation of Built-in Self-Repair Architectures for Random Logic SoC Cores
  Roland Dobai, Marcel Balaz and Maria Fischerova
- Miscellaneous Types of Partial Duplication Modifications for Availability Improvements
  Jaroslav Borecký, Martin Kohlík and Hana Kubátová
- Reliability of Task Execution during Safe Software Processing
  Peter Raab, Stanislav Racek, Juergen Mottok and Stefan Krämer

ET – 1: Important Issues Introduced by Emerging Technologies

Location: Gerence 2

Chair: D. Quaglia

- Power Optimization Opportunities for a Reconfigurable Arithmetic Component in the Deep Submicron Domain
  Dimitris Bekiaris and George Economakos
- OWQS: One-Way Quantum Computation Simulator
  Eesa Nikahd, Mahboobeh Houshmand, Morteza Saheb Zamani and Mehdi Sedighi

EPDSD – 1: European Projects in DSD

Location: Gerence 3

Chair: L. Jozwiak

- The ACROSS MPSoC – A New Generation of Multi-Core Processors designed for Safety-Critical Embedded Systems
  Christian El Salloum, Martin Elshuber, Oliver Höftberger, Haris Isakovic and Armin Wasicek
- From Scilab To High Performance Embedded Multicore Systems – The ALMA Approach
  Juergen Becker, Michael Huebner, Timo Stripf, Steven Derrien, Daniel Menard, Olivier Sentieys, Gerard Rauwerda, Kim Sunesen, Nikolaos Kavvadias, Kostas Masselos, George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Dimitrios Kritharidis, Nikolaos Mitas and Diana Goehringer

16:00 – 16:30 Coffee Break

Location: Foyer

16:00 – 16:30 Poster Session – 1

Location: Ballroom

- FPGA based Real-Time Tracking Approach with Validation of Precision and Performance
  Alexander Bochem, Kenneth Kent and Rainer Herpers
- Analyzing Bus Load Data Using an FPGA and a Microcontroller
  Marcel Dombrowski, Kenneth B. Kent, Yves Losier, Adam Wilson and Rainer Herpers
- On the Development of a Runtime Reconfigurable Multicore System-on-Chip
  Andrea Cazzaniga, Gianluca Durelli, Christian Pilato, Donatella Sciuto and Marco Domenico Santambrogio
- Resilient Adaptive Algebraic Architecture for Parallel Detection and Correction of Soft-Errors
  Fabio Itturriet, Ronaldo Ferreira, Gustavo Girao, Gabriel Nazar, Alvaro Moreira and Luigi Carro
- Improving the Soft Error Resilience of the Register Files Using SRAM Bitcells with Built-in Comparators
  Mehmet Kayaalp, Fahrettin Koc and Oguz Ergin
- Vulnerability Analysis For Custom Instructions
  Ali Azarpeyvand, Mostafa Ersali Salehi Nasab and Seid Mehdi Fakhraie
- A Three-Dimensional Integrated Accelerator
  Farhad Mehdipour, Krishna C. Nunna, Koji Inoue and Kazuaki J. Murakami
- Using Algorithm Parallelism Estimation to Constrain Instruction-Set Synthesis for VLIW Processors
  Roel Jordans, Rosilde Corvino and Lech Jozwiak

16:30 – 18:00 Sessions

AHSA – 1: Architectures and Hardware for Security Applications

Location: Ballroom

Chair: P. Kitsos

- An Easy-to-Design PUF based on a single oscillator: the Loop PUF
  Zouha Cherif, Jean Luc Danger, Sylvain Guilley and Lilian Bossuet
- No Principal Too Small: Memory Access Control for Fine-Grained Protection Domains
  Eugen Leontie, Gedare Bloom, Bhagirath Narahari and Rahul Simha
- Hardware Strengthening a Distributed Logging Scheme
  Jo Vliegen, Karel Wouters, Christian Grahn and Tobias Pulls
- Trojan Immune Circuits Using Duality
  Yousra Alkabani

MORPS – 2: Monitoring and Reconfiguration of Parallel Systems

Location: Gerence 2

Chair: E. Nigussie

- Semi-distributed control for FPGA-based reconfigurable systems
  Chiraz Trabelsi, Samy Meftali and Jean-Luc Dekeyser
- FPGA-Based Neural Network for Nonuniformity Correction on Infrared Focal Plane Arrays
  Nicolas Celedon, Rodolfo Redlich and Miguel Figueroa
- MAFA: Adaptive Fault-Tolerant Routing Algorithm for Networks-on-Chip
  Masoumeh Ebrahimi, Masoud Daneshtalab and Juha Plosila
- Power and Thermal Analysis of Stacked Mesh 3D NoC Using AdaptiveXYZ Routing Algorithm
  Amir-Mohammad Rahmani, Kameswar Rao Vaddina, Pasi Liljeberg, Juha Plosila and Hannu Tenhunen.

EPDSD – 2: European Projects in DSD

Location: Gerence 3

Chair: F. Leporati

- ASAM: Automatic Architecture Synthesis and Application Mapping
  Lech Jozwiak, Menno Lindwer, Rosilde Corvino, Paolo Meloni, Laura Micconi, Jan Madsen, Erkan Diken, Deepak Gangadharan, Roel Jordans, Sebastiano Pomata, Paul Pop, Giuseppe Tuveri and Luigi Raffo
- Controlling Hardware Synthesis with Aspects
  João M.P. Cardoso, Tiago Carvalho, José G.F. Coutinho, Pedro Diniz, Zlatko Petrov and Wayne Luk
- FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration
  Dionisios Pnevmatikatos, Tobias Becker, Andreas Brokalakis, Karel Bruneel, Georgi Gaydadjiev, Wayne Luk, Kyprianos Papadimitriou, Ioannis Papaefstathiou, Oliver Pell, Christian Pilato, Mathieu Robart, Marco Santambrogio, Donatella Sciuto, Dirk Stroobandt and Tim Todman

Thursday, 6 September 2012

8:30 – 9:00 Registration

9:00 – 10:00 Keynote Speech – 3 (DSD - 2)

Location: Ballroom

- Multicore Platform Design: Tackling a Grand Challenge in Embedded Computing
  Rainer Leupers

10:00 – 10:30 Coffee Break

Location: Foyer

10:30 – 12:30 Sessions

FTDSD – 3: Fault Tolerance in Digital System Design

Location: Ballroom

Chair: R. Dobai

- Energy-aware Fault-tolerant Network-on-chips for Addressing Multiple Traffic Classes
  Syed Mohammad Asad Hassan Jafri, Liang Guang, Ahmed Hemani, Juha Plosila, Kolin Paul and Hannu Tenhunen
- Dependability Analysis of Fault Tolerant Systems Based on Partial Dynamic Reconfiguration Implemented into FPGA
  Jan Kastil, Martin Straka, Lukas Miculka and Zdenek Kotasek
- Activity Migration in M-of-N-Systems by means of Load-Balancing
  Markus Ulbricht, Heinrich Theodor Vierhaus and Tobias Koal
- Protecting an Asynchronous NoC against Transient Channel Faults
  Syed Rameez Naqvi, Varadan Savulimedu Veeravalli and Andreas Steininger
- On Distribution and Impact of Fault Effects at Real-Time Kernel and Application Levels
  Josef Strnadel and Frantisek Slimarik
- Exploiting Bus Level and Bit Level Inactivity for Preventing Wire Degradation due To Electromigration
  Mehmet Kayaalp, Fahrettin Koc and Oguz Ergin

SoC&NoC – 1: Systems and Networks on Chip

Location: Gerence 2

Chair: O. Ozturk

- A Heuristic Energy-Aware Approach for Hard Real-Time Systems on Multi-Core Platforms
  [Best Paper Candidate]

Da He and Wolfgang Mueller

- ONC3: All-Optical NoC based on Cube-Connected Cycles with Quasi-DOR Algorithm
  [Best Paper Candidate]
  Meisam Abdollahi, Mohammad Khavari Tavana, Somayyeh Koohi and Shaahin Hessabi
- Architecture Support and Comparison of Three Memory Consistency Models in NoC based Systems
  Abdul Naeem, Axel Jantsch and Zhonghai Lu
- A Simple On-chip Optical Interconnection for Improving Performance of Coherency Traffic in CMPs
  Sandro Bartolini and Paolo Grani
- High Speed Dynamic Partial Reconfiguration for Real Time Multimedia Signal Processing
  Francesco Bruschi, Marco Domenico Santambrogio, Paolo Roberto Grassi and Sheetal Bhandari

EPDSD – 3: European Projects in DSD

Location: Gerence 3

Chair: E. Villar

- The Seat Adaptation System of REFLECT Project: Implementation of a Byocibernetic Loop in an Automotive Environment
  Gian Mario Bertolotti, Andrea Cristiani, Remo Lombardi and Nikola Serbedzija
- The DeSyRe project: on-Demand System Reliability
  Ioannis Sourdis, Christos Strydis, Christos-Savvas Bouganis, Babak Falsafi, Georgi N. Gaydadjiev, Alirad Malek, Riccardo Mariani, Dionisios N. Pnevmatikatos, Dhiraj K. Pradhan, Gerard Rauwerda, Kim Sunesen and Stavros Tzilis
- FASTCUDA: Open Source FPGA Accelerator & Hardware-Software Codesign Toolset for CUDA Kernels
  Iakovos Mavroidis, Ioannis Mavroidis, Ioannis Papaefstathiou and Luciano Lavagno
- COMPLEX - COdesign and power Management in PLatform-based design space Exploration
  Kim Gruttner, Philipp Hartmann, Kai Hylla, Sven Rosinger, Carlo Brandolese, William Fornaciari, Gianluca Palermo, Davide Quaglia, Wolfgang Nebel, Chantal Ykman-Couvreur, Francisco Ferrero, Raul Valencia, Fernando Herrera and Eugenio Villar

12:30 – 13:30 Lunch Break

13:30 – 14:30 Keynote Speech – 4 (DSD - 3)

Location: Ballroom

- Tech and Space, A Symbiotic Relationship
  Rich Goldman, ***Synopsys, Inc.***

14:30 – 15:30 Sessions

DTDS – 1: Dependability and Testing of Digital Systems

Location: Ballroom

Chair: H. Kubátová

- Using Genetic Algorithm to Identify Soft-Error Derating Blocks of an Application Program
  Bahman Arasteh, Ali Mansoor, Seyed Ghassem Miremadi, and Amir Masoud Rahmani
- The Influence of Implementation Technology on Dependability Parameters
  Jan Schmidt, Petr Fiser and Jiří Balcárek

ET – 2: Important Issues Introduced by Emerging Technologies

Location: Gerence 2

Chair: F. Mehdipour

- TSV-Virtualization for Multi-Protocol-Interconnect in 3D-ICs
  Felix Miller, Thomas Wild and Andreas Herkersdorf
- A Methodology for Early Exploration of TSV Placement Topologies in 3D Stacked ICs
  Radhika Jagtap, Sumeet S. Kumar and Rene Van Leuken

SHES – 2: System, Hardware and Embedded Software Design and Automatic Synthesis

Location: Gerence 3

Chair: I. Sourdis

- Multi-Device Driver Synthesis Flow for Heterogeneous Hierarchical Systems
  Alexandre Chagoya-Garzon, Frédéric Pétrot and Frederic Rousseau
- A Verifiable High Level Data Path Synthesis Framework
  Görker Alp Malazgirt, Ender Culha, Alper Sen, Faik Baskaya and Arda Yurdakul
- Finite State Machine Synthesis Based on Relay-Based algorithm
  Meng Yang

15:30 – 16:00 Coffee Break

Location: Foyer

15:30 – 16:00 Poster Session – 2

Location: Ballroom

- VLSI Reverse Converter for RNS based on the Moduli Set {2^n+1, 2^n-1, 2^{2n+1}-3, 2^{2n}-2}
  Leonel Sousa and Samuel Antao
- EJOP: an Extensible Java Processor with Reasonable Performance/Flexibility Trade-off
  Samaneh Talebi, Ali Jahanian and Niloofar Abolghasemi
- A dual-core coprocessor with native 4D Clifford algebra support
  Silvia Franchini, Antonio Gentile, Giorgio Vassallo, Salvatore Vitabile and Filippo Sorbello

- SystemC model generation for realistic simulation of networked embedded systems
  Parinaz Sayyah, Francesco Stefanni, Luciano Lavagno and Davide Quaglia
- How to Prove that a Circuit is Fault-Free?
  Raimund Ubar, Sergei Kostin and Jaan Raik
- On Modeling and Evaluation of Logic Circuits Under Timing Variations
  Mehdi Dehbashi, Görschwin Fey, Kaushik Roy and Anand Raghunathan

16:00 – 18:00 Sessions

FDR: Flexible Digital Radio

Location: Ballroom

Chair: D. Noguet

- IEEE 802.11p Receiver Design for Software Defined Radio Platforms
  Carina Schmidt-Knorreck, Daniel Knorreck and Raymond Knopp
- Analytical Design Space Exploration based on statistically Refined Runtime and Logic Estimation for Software Defined Radios
  Matthias Ihmig, Michael Feilen and Andreas Herkersdorf
- HDCRAM Proof-of-Concept for Opportunistic Spectrum Access
  Oussama Lazrak, Pierre Leray and Christophe Moy
- A Flexible Hardware Platform for Mobile Cognitive Radio applications
  Vincent Berg, Dominique Noguet and Xavier Popon
- Flexible OFDM waveform for PLC/RF in-vehicle communications
  Fabienne Nouvel and Philippe Tanguy

DHCPS: Design of Heterogeneous Cyber-Physical Systems

Location: Gerence 2

Chair: D. Quaglia

- Open Problems in Verification and Refinement of Autonomous Robotic Systems
  Davide Bresolin, Luigi Di Guglielmo, Luca Geretti, Riccardo Muradore, Paolo Fiorini and Tiziano Villa
- Cyber-Physical Systems Design for Electric Vehicles
  Martin Lukasiewycz, Sebastian Steinhorst, Florian Sagstetter, Wanli Chang, Peter Waszecki, Matthias Kauer and Samarjit Chakraborty
- Simulation-based analysis of cyberphysical systems
  Masahiro Fujita
- Model Checking on Hybrid Automata: Theory and Application to Biological Systems
  Alberto Casagrande, Carla Piazza and Carla Piazza

EPDSD – 4: European Projects in DSD

Location: Gerence 3

Chair: F. Leporati

- Apple-CORE: Microgrids of SVP cores
  Raphael Poss, Mike Lankamp, Chris Jesshope, Michiel W. van Tol, Qiang Yang and Jian Fu
- HEAP: a Highly Efficient Adaptive multi-Processor framework
  Luciano Lavagno, Mihai Lazarescu, Johan Walters, Bart Kienhuis, Ioannis Papaefstathiou, Andreas Brokalakis and Florian Schäefer
- System Adaptivity and Fault-tolerance in NoC-based MPSoCs: the MADNESS Project Approach
  Paolo Meloni, Giuseppe Tuveri, Luigi Raffo, Emanuele Cannella, Todor Stefanov, Onur Derin, Leandro Fiorin and Mariagiovanna Sami

Friday, 7 September 2012

8:30 – 9:00 Registration

9:00 – 10:00 Keynote Speech – 5 (SEAA- 2)

Location: Ballroom

- Things aren't always what they seem: Three examples of seemingly proper statistical analyses leading to unsubstantiated software engineering claims
  Magne Jørgensen

10:00 – 10:30 Coffee Break

Location: Foyer

10:00 – 10:30 Poster Session – 3

Location: Ballroom

- Coverage-driven Stimuli Generation
  Shuo Yang, Robert Wille, Daniel Grosse and Rolf Drechsler
- Convolutional Decoding on Deep-pipelined SIMD Processor with Flexible Parallel Memory
  Jian Wang, Andreas Karlsson, Joar Sohl and Dake Liu
- Evaluation of the Hardware Performance Space of SHA-3 Candidates Blue Midnight Wish and CubeHash using FPGAs
  Robert Lorentz and Kris Gaj
- Hardware Acceleration of STON Algorithm for Comparing 3-D Structure of Proteins
  Somayeh Kashi and Morteza Sahebzamani
- High Level Modeling and Simulation of a Baseband Processor for the 60 GHz Band
  Ruben Cabral and Helena Sarmento
- A virtual platform for performance estimation of many-core implementations
  Pablo González De Aledo, Javier González-Bayón and Pablo Sanchez
- Open-People: Open-Power and Energy Optimization Platform and Estimator
  E. Senn, C.Belleudy, D.Chillet, A.Fritsch, R.Ben Atitallah and O.Zendra

10:30 – 12:30 Sessions

AHSA – 2: Architectures and Hardware for Security Applications

Location: Ballroom

Chair: P. Kitsos

- Differential Scan Attack on AES with X-Tolerant and X-Masked Test Response Compactor
  Amitabh Das, Baris Ege, Santosh Ghosh and Ingrid Verbauwhede

- A Parallel Architecture for Koblitz Curve Scalar Multiplications on FPGA Platforms
  Sujoy Sinha Roy, Chester Rebeiro and Debdeep Mukhopadhyay
- Evaluating Cryptanalytical Strength of Lightweight Cipher PRESENT on Reconfigurable Hardware
  Jan Pospisil and Martin Novotny
- A High-Speed Unified Hardware Architecture for the AES and SHA-3 Candidate Gr{\o}stl
  Marcin Rogawski and Kris Gaj

SoC&NoC – 2: Systems and Networks on Chip

Location: Gerence 2

Chair: B.Juurlink

- Minimizing Power Consumption of Spatial Division based Networks-on-Chip Using Multi-Path and Frequency Reduction
  Sheng Hao Wang, Anup Das, Akash Kumar and Henk Corporaal
- Optimal 2D Data Partitioning for DMA Transfers on MPSoCs
  Selma Saidi, Oded Maler, Pranav Tendulkar and Thierry Lepley
- Distance-Constrained Force-Directed Process Mapping for MPSoC Architectures
  Timo Schönwald, Alexander Viehl, Oliver Bringmann and Wolfgang Rosenstiel
- Reducing Instruction Issue Overheads in Application Specific Vector Processors
  Jaroslav Sykora, Roman Bartosinski, Lukas Kohout, Martin Danek and Petr Honzik

APP – 1: Applications of (Embedded) Digital Systems

Location: Gerence 3

Chair: D.Chillet

- Partitioning and Assignment Exploration for Multiple Modes of IEEE 802.11n Modem on Heterogeneous MPSoC Platforms
  Prashant Agrawal, Kanishk Sugand, Martin Palkovic, Praveen Raghavan, Liesbet Van der Perre and Francky Catthoor
- Adaptive Field Strength Scaling - A Power Optimization Technique for Contactless Reader / Smart Card Systems
  Norbert Druml, Manuel Menghin, Christian Steger, Reinhold Weiss, Andreas Genser, Holger Bock and Josef Haid
- RF-Interconnect Resource Assignment and Placement Algorithms in Application Specific ICs to Improve Performance and Reduce Routing Congestion
  Bahareh Pourshirazi and Ali Jahanian
- High Performance Unified Architecture for Forward and Inverse Quantization in H.264/AVC
  Tiago Dias, Luís Rosário, Nuno Roma and Leonel Sousa

12:30 – 13:30 Lunch Break

13:30 – 15:00 Sessions

AHSA – 3: Architectures and Hardware for Security Applications

Location: Ballroom

Chair: F. Leporati

- JAAVR: Introducing the Next Generation of Security-enabled RFID Tags
  Erich Wenger, Thomas Baier and Johannes Feichtner
- FPGA-based Design Approaches of Keccak Hash Function
  George Provelengios, Paris Kitsos, Nicolas Sklavos and Christos Koulamas
- PROCOMON - An Automatically Generated Predictive Control-Signal Monitor
  Armin Krieg, Johannes Grinschgl, Norbert Druml, Christian Steger, Holger Bock and Josef Haid
- CRT RSA Hardware Architecture with Fault and Simple Power Attack Countermeasures
  Apostolos Fournaris and Odysseas Koufopavlou

SLEO-WSN – 1: System Level Energy Optimization and Wireless Sensor Networks

Location: Gerence 2

Chair: P. Sanchez

- Open-People: Open-Power and Energy Optimization Platform and Estimator
  E. Senn, C.Belleudy, D.Chillet, A.Fritsch, R.Ben Atitallah and O.Zendra
- An Hardware-In-the-Design Methodology for Wireless Sensor Networks based on Event-Driven Impulse Radio Ultra-Wide Band
  Alberto Bonanno, Alessandro Sanginario, Marco Crepaldi and Danilo Demarchi
- Energy characterization and classification of embedded operating system services
  Bassem Ouni, Cecile Belleudy and Eric Senn

SMVT: System, Hardware and Embedded Software Specification, Modeling, Verification and Test

Location: Gerence 3

Chair: A.M. Molnos

- Enhanced IP-XACT Platform Descriptions for Automatic Generation from UML/MARTE of Fast Performance Models for DES
  Fernando Herrera, Héctor Posadas, Eugenio Villar and Daniel Calvo
- Automated Generation of Embedded Systems Software from timed DEVS Model of Computation Specifications
  H. Gregor Molter, Johannes Kohlmann and Sorin A. Huss
- Generation of VHDL code from UML/MARTE sequence diagrams for verification and synthesis
  Emad Samuel Malki Ebeid, Franco Fummi and Davide Quaglia
- Extending MARTE to support the specification and the generation of data-intensive applications for Massively Parallel SoC
  Manel Ammar, Mouna Baklouti and Mohamed Abid

WiP/Ph.D. – 1: Work in Progress / Ph.D. Symposium

Location: Deniz Kızı 3

Chair: Radu Calinescu, K. Kloeckner, K.E Grosspietsch

- Cost-Efficient Resource Allocation for Multi-tier Web Applications in a Cloud Environment
  Adnan Ashraf
- Goal-Business Process Integration through Choreography within Enterprise Architecture
  Cahit Gungor
- Measuring Software Engineer Motivation in Globally Distributed Projects
  Liva Šteinberga
- QoS-enabled Middleware for Smart Grids
  Abdel Rahman, Alkhavaja, Luis Lino Ferreira, Michele Albano, Ricardo Garibay
- A Proposal for Multidisciplinary Software for People with Autism
  Eraldo Guerra, Felipe Furtado
- Discussion: What are the challenges of doing a PhD in Software Engineering?

15:00 – 15:30 Coffee Break

Location: Foyer

15:00 – 15:30 Poster Session – 4

Location: Ballroom

- Managing a Massively-Parallel Resource-Constrained Computing Architecture
  Cameron Patterson, Thomas Preston, Francesco Galluppi and Steve Furber
- Evaluation of a Connectionless NoC for a Real-Time Distributed Shared Memory Many-Core System
  Jochem H. Rutgers, Marco J.G. Bekooij and Gerard J.M. Smit
- CoolMap: A Thermal-Aware Mapping Algorithm For Application Specific Networks-on-Chip
  Mostafa Moazzen, Akram Reza and Midia Reshadi
- Efficient DPA-Resistance Verification Method with Smaller Number of Power Traces on AES Cryptographic Circuit
  Hiroki Ito, Mitsuru Shiozaki, Anh-Tuan Hoang and Takeshi Fujino
- A Distributed Feedback Control Mechanism for Quality-of-Service Maintenance in Wireless Sensor Networks
  Marcel Steine, Marc Geilen and Twan Basten

15:30 – 17:30 Sessions

MSDA: Multicore Systems: Design and Applications

Location: Gerence 1

Chair: H. Corporaal

- MAMOT: Memory-Aware Mapping Optimization Tool for MPSoC

Olivera Jovanovic, Iuliana Bacivarov, Peter Marwedel and Lothar Thiele

- OpenMP-based Synergistic Parallelization and HW Acceleration for On-Chip Shared-Memory Clusters
  Paolo Burgio, Andrea Marongiu, Dominique Heller, Cyrille Chavet, Philippe Coussy and Luca Benini
- A Game Theoretical Thermal–Aware Run–Time Task Synchronization Method for Multiprocessor Systems–on–Chip
  Yasar Asgarieh, Mohammad Khabbazian, Mehdi Modarressi and Hamid Sarbazi-Azad
- Composable Virtual Memory for an Embedded SoC
  Cor Meenderinck, Anca Molnos and Kees Goossens
- Transformation-based Exploration of Data Parallel Architecture for Customizable Hardware: A JPEG Encoder Case Study
  Rosilde Corvino, Erkan Diken, Abdoulaye Gamatie and Lech Jozwiak

SHES – 3: System, Hardware and Embedded Software Design and Automatic Synthesis

Location: Deniz Kızı 2

Chair: A.Yurdukal

- Efficient Parallel Decimal Multipliers and Squarers using Karatsuba-Ofman's Algorithm
  Mário Véstias and Horacio Neto
- The Synthesis of Combined Mealy and Moore Machines Structural Model Using Values of Output Variables as Codes of States
  Adam Klimowicz and Valery Soloviev
- RNS Arithmetic Units for \textit{Modulo} $\{2^n \pm k\}$
  Pedro Miguens Matutino, Hector Pettenghi, Ricardo Chaves and Leonel Sousa
- Scalability Study of Polymorphic Register Files
  Catalin Bogdan Ciobanu, Georgi Kuzmanov and Georgi Gaydadjiev
- Pipelined Large Multiplier Designs on FPGAs
  Ali Senturk and Mustafa Gok
- Implementation Study of FFT on Multi-Lane Vector Processors
  Bogdan Spinean and Georgi Gaydadjiev

DTDS – 2: Dependability and Testing of Digital Systems

Location: Ballroom

Chair: H. Kubátová

- Robust Evaluation of Weighted Random Logic BIST Structures in Industrial Designs
  René Krenz-Baath, Friedrich Hapke, Rolf Hinze, Andreas Glowatz, Reinhard Meier and Maija Ryynaenen
- Test Generation Approach for Post-Silicon Validation of High End Microprocessor
  Satish Kumar Sadasivam, Sangram Alapati, Varun Mallikarjunan and Prathiba Kumar

- Investigating Dependability of Short-Range Wireless Embedded Systems through Hardware Platform based Design
  Benaoumeur Senouci, Anne Johan Annema, Mark Bentum and Hans Kerkhoff
- Scan Based Tests Via Standard Interfaces
  Christian Gleichner and H.T. Vierhaus
- Soft Error Analysis on Communication Channels in On-Chip Communication Networks
  Mohammadreza Najafi, Saeed Safari and Zainalabdein Navabi

SLEO-WSN – 2: System Level Energy Optimization and Wireless Sensor Networks

Location: Gerence 2

Chair: T. Basten

- Virtual Platform for Wireless Sensor Network
  Alvaro Diaz Suarez, Raul Diego and Pablo Sanchez
- Energy-Aware FPGA-Based Architecture for Wireless Sensor Networks
  Paolo Roberto Grassi and Donatella Sciuto
- Tacit Consent: A Technique to Reduce Redundant Transmissions from Spatially Correlated Nodes in Wireless Sensor Networks
  Paolo Roberto Grassi, Ivan Beretta, Vincenzo Rana and Donatella Sciuto
- A Novel Predictor-based Power-Saving Policy for DRAM Memories
  Gervin Thomas, Karthik Chandrasekar, Benny Akesson, Ben Juurlink and Kees Goossens
- Evaluation of an FPGA-based Reconfigurable SoC for All-Digital Flexible RF Transmitters
  Nelson Silva, Arnaldo Oliveira and Nuno Carvalho
- Design and Implementation of a Circuit for Mesh Networks with Application in Body Area Networks
  Fardin Derogarian, João Canas Ferreira and Vítor M. Grade Tavares

APP – 2: Applications of (Embedded) Digital Systems

Location: Gerence 3

Chair: I. Hamzaoglu

- H.264 Macroblock Line Level Parallel Video Decoding on Embedded Multicore Processors
  Elias Baaklini, Hassan Sbeity and Smail Niar
- Enhanced Omnidirectional Image Reconstruction Algorithm and its Real-Time Hardware
  Abdulkadir Akin, Elif Erdede, Hossein Afshari, Alexandre Schmid and Yusuf Leblebici
- A Small and High-performance Coprocessor for Fingerprint Match-On-Card
  Taoufik Chouta, Jean-Luc Danger, Laurent Sauvage and Tarik Graba
- On-Package Scalability of RF and Inductive Memory Controllers
  Mario Donato Marino
- A hardware accelerator for real time simulation of complex neuronal models
  Alessandra Majani, Maria Chiara Lorena, Francesco Leporati and Giovanni Danese
- Design of High-Speed Viterbi Decoders on Virtex-6 FPGAs

Mário Véstias, Horacio Neto and Helena Sarmento

WiP/Ph.D. – 2: Work in Progress / Ph.D. Symposium

Location: Deniz Kızı 3

Chair: Radu Calinescu, K. Kloeckner, K.E Grosspietsch

- Error-Resilient BDDs: A Preliminary Study
  Lorenzo Lago, Anna Bernasconi, Valentina Ciriani
- A Haskell-Based Programming Paradigm for Coarse-Grained Reconfigurable Arrays
  Anja Niedermeier, Jan Kuper, Gerard Smit
- High Breakdown Voltage and Switching Speed IGBT Design
  A. Belous, I. Lovshenko, V. Nelayev, A. Turtsevich, I. Shelibak
- Design Methodology for Implementing Multiplexer Based Ternary Logic Circuits Using Carbon Nanotube Field Effekt Transistor (CNFET)
  Chetan Vudadha, P. Sai Phaneendra, V. Sreehari, M.B. Srinivas
- Algorithmic vs Architectural Optimizations in a C-Based PLC to FPGA Translation Environment
  Christoforos Economakos, George Economakos
- Visual Exploration of Changing FPGA Architectures in the VTR Project
  Konstantin Nasartschuk, Kenneth B. Kent, Rainer Herpers
- Design Synchronization after Partial Dynamic Reconfiguration of Fault Tolerant System
  Lukas Miculka, Zdenek Kotasek
- Analysis Approach for Safefy Critical Hardware using Neural Networks
  M. Schmedes, A. Th. Schwarzbacher, B. Hoppe

17:30 – 18:00 Closing

Location: Ballroom